In the Claims

Please cancel claims 1-25, without prejudice or disclaimer.

26. (Original) An NMOS transistor having an improved narrow width Vt roll-off, comprising:

(a) a substrate that includes shallow trench isolation (STI) features which are comprised of a shallow trench with sloped sidewalls and a bottom, an oxide liner formed on said shallow trench sidewalls and bottom, and an insulator layer formed on said oxide liner that fills said shallow trench and extends to a level that is above the top of said substrate;

(b) an active area formed between two adjacent shallow trenches in said substrate; said active area having an indium doped region that is adjacent to top corners of said shallow trenches;

(c) a gate dielectric layer formed on said active area; and

(d) a patterned gate layer formed on said fate dielectric layer wherein said gate layer extends over said adjacent shallow trenches.

27. (Original) The NMOS transistor of claim 26 wherein said substrate is also comprised of a second p-type dopant in said active areas.

28. (Original) The NMOS transistor of claim 26 wherein the depth of said shallow trench is about 1500 to 5000 Angstroms and the width of the shallow trench ranges from less than 100 nm to several microns.

29. (Original) The NMOS transistor of claim 26 wherein said oxide liner has a thickness of about 50 to 300 Angstroms.

30. (Original) The NMOS transistor of claim 26 wherein said insulator layer is comprised of SiO_2 or a low k dielectric material.

31. (Original) The NMOS transistor of claim 26 wherein said doped idium region has an idium concentration from about 10^{14} to 10^{19} ions/cm^3 and has a thickness in the range of about 30 to 1000 Angstroms.

32. (Original) The NMOS transistor structure of claim 26 wherein said idium doped region extends away from said shallow trench to a distance between 0 and about 1000 Angstroms.

33. (Original) The structure of claim 26 wherein said gate dielectric layer is comprised of SiO_2 or an upper high k dielectric metal oxide layer on a lower interfacial layer.

34. (Original) The NMOS transistor of claim 26 wherein said gate layer has a thickness of about 300 to 5000 Angstroms and forms a conformal layer on said gate dielectric layer and on said adjacent STI features.

35. (Original) The structure of claim 26 wherein said gate layer is comprised of doped polysilicon.

36. (Original) The NMOS transistor of claim 26 wherein said gate layer is comprised of undoped polysilicon or amorphous silicon.